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REMARKS

Applicants have amended their claims in order to further clarify the definition of the present invention. Specifically, Applicants have amended claims 30 and 32 to recite a plurality of insulated-gate semiconductor elements, rather than a plurality of insulated-gate "type" semiconductor elements. Applicants have also amended claim 32 to recite that "a portion of" the semiconductor thin-film layer located between the semiconductor elements is provided with a bottle-neck region of which cross-sectional area is smaller than that of other portions "of said semiconductor thin-film layer".

Moreover, Applicants have canceled claims 1-3, 16-18 and 34 without prejudice or disclaimer.

Applicants have set forth the subject matter of claim 11 in independent form, as new claim 37; and in light of new claim 37, have canceled claim 11 without prejudice or disclaimer.

In addition to claim 37, Applicants are adding new claims 35 and 36 to the application. Claim 35, dependent on claim 30, recites specified metals, alloys and compounds from which the seed crystal metal is selected. Claim 36, dependent on claim 4, recites that the gate region includes a gate electrode, and that the gate electrode is made of a metal.

Applicants respectfully traverse the rejection of claims 30 and 31 under the second paragraph of 35 USC 112, as set forth in Item 3 on pages 2 and 3 of the Office Action mailed May 1, 2002, especially insofar as applicable to the claims as presently amended. Contrary to the conclusion by the Examiner, it is respectfully submitted that claims 30 and 31 are not incomplete and do not omit essential structural cooperative relationships of elements, as contended by the Examiner.

That is, note that claim 30 defines that the integrated circuit device includes a plurality of insulated-gate semiconductor elements formed at the semiconductor thin-film layer, each having a gate electrode separated from the semiconductor thin-film layer by a gate insulating film. Clearly, this appropriately defines structure of the semiconductor elements, in that, for example, an insulated-gate semiconductor element includes a gate electrode separated from the semiconductor thin-film layer by a gate insulating film. It is noted that claim 30 further recites a seed crystal metal located between at least two of the gate insulating films and provided on the surface of the semiconductor thin-film layer. This seed crystal metal, as defined in Applicants' disclosure, is a different component than the gate electrode, and is provided in order to achieve desired crystallization of the semiconductor thin-film layer and retained in the structure formed. Clearly, the seed crystal metal is to be provided on the surface of the semiconductor thin-film layer, according to various aspects of the present invention, in order to provide the necessary seed for the crystallization.

The contention by the Examiner in the paragraph bridging pages 2 and 3 of the Office Action mailed May 1, 2002, that gate-type elements formed at the semiconductor thin-film layer is inconsistent with the gate electrode being separated from the semiconductor thin-film layer by a gate insulating film, is respectfully traversed. As presently amended, the claims recite a plurality of insulated-gate semiconductor elements formed at the semiconductor thin-film layer, which is consistent with these elements having a gate electrode separated from the semiconductor thin-film layer by a gate insulating film, while the elements are formed at the semiconductor thin-film layer in that, semiconductor active regions are provided within the semiconductor thin-film layer.

The comment by the Examiner in the first two lines on page 3 of the Office Action mailed May 1, 2002, that it is not clear if the "elements" are the gates themselves or other structures associated with the gates, is noted. As presently amended, claim 30 recites insulated-gate semiconductor elements, with each of these elements having a gate electrode. It is respectfully submitted that, particularly as presently amended, the claims are clear that the elements are not the gate electrodes themselves, but rather are, for example, semiconductor devices (e,g., insulated-gate field effect transistors; illustratively and not to be limiting).

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in the Office Action mailed May 1, 2002, that is, the teachings of the U.S. patent to Yamazaki, et al., No. 6,348,368, and to Owyang, et al., No. 6,060,375, under the provisions of 35 USC 102 and 35 USC 103.

Initially, it is noted that claims 1-3 and 34 have been canceled without prejudice or disclaimer. Accordingly, the rejection of claims 1-3 and 34 under 35 USC 102(a), set forth on page 3 of the Office Action mailed May 1, 2002, is moot.

In addition, it is noted that claim 11 was objected to as being dependent upon a rejected base claim, but it was indicated that claim 11 would be allowable if rewritten in independent form. Claim 11 has now been rewritten in independent form as new claim 37. Thus, claim 37 should now be allowed.

As for the remaining claims, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such a thin-film semiconductor device as in the present claims, having the polycrystalline layer formed on an insulator, with this polycrystalline layer including crystal grains of an element selected from the group Type-IV elements and the alloys thereof, and

with the crystal grains joined with crystal grain boundaries of {111} twin of Diamond structure. See claim 4; note also, e.g., claim 33.

In addition, it is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a thin-film semiconductor device as in the present claims, having the semiconductor thin-film formed on the insulator and a transistor including, inter alia, a gate electrode formed at the surface of the semiconductor thin-film, with the semiconductor thin-film having, inter alia, dendrite crystal regions of Type-IV element connecting the source region and the drain region. See claim 9.

Furthermore, it is respectfully submitted that these applied references would have neither taught nor would have suggested such a thin-film semiconductor integrated circuit device as in the present claims, having the plurality of insulated-gate semiconductor elements, with each of the elements having a gate electrode, the device having a seed crystal metal located between at least two of the gate insulating films and provided on the surface of the semiconductor thin-film layer except for the areas just under the gate insulating films of each of the semiconductor elements. See claim 30.

In addition, it is respectfully submitted that these applied references would have neither taught nor would have suggested such a thin-film semiconductor integrated circuit device as in the present claims, having the plurality of insulated-gate semiconductor elements formed at the semiconductor thin-film layer, wherein a portion of the thin-film layer located between the semiconductor elements is provided with a bottle-neck region of which cross-sectional area is smaller than that of other portions of the semiconductor thin-film layer. See claim 32.

Moreover, it is respectfully submitted that the teachings of these applied

references would have neither disclosed nor would have suggested such a thin-film semiconductor device as in the present claims, and including the additional features of the present invention as in the remaining, dependent claims, including (but not limited to) wherein the gate region includes a gate electrode made of a metal (see claim 36); and/or wherein, in at least one current path connecting the source and drain regions, at least one of the crystal grain boundaries crossing the current path is the {111} twin of Diamond structure (note, for example, claims 7 and 10); and/or wherein in the channel region there are 2 to 5 crystal grains having the joints of the {111} twin, which have {110} planes parallel to the surface of the insulator (note claims 7 and 12); and/or metals of the seed crystal, as in claims 28 and 35.

The present invention, as being considered in the above-identified application, is directed to a thin-film semiconductor device (for example, a thin-film semiconductor integrated circuit device). Such device is useful, for example, in a liquid crystal display device.

Thin film transistors are used in image display devices, for example, and in such structures polycrystalline silicon is formed on a quartz substrate through a high-temperature heat treatment to provide polycrystals of silicon of comparatively large grain size. A thin film transistor formed using this high-temperature polycrystalline silicon has a lower density of grain boundary and good crystallinity in the channel region, making it possible to obtain relatively high electron mobility. However, this high-temperature polycrystalline silicon requires use of an expensive quartz substrate which tolerates the high-temperature processing, so that it has been difficult to reduce the total cost of the structure formed.

Recently, low-temperature polycrystalline silicon has been investigated in place of the high-temperature polycrystalline silicon. In forming the low-temperature

polycrystalline silicon, amorphous silicon or microcrystalline silicon is formed on a low-cost glass substrate using a plasma chemical vapor deposition method or the like, which silicon is then crystallized with a melt-grown method using, for example, a laser anneal. However, the existing low-temperature polycrystalline silicon has smaller grain size than that of the high-temperature polycrystalline silicon, and thin-film transistors using this low-temperature polycrystalline silicon have large carrier scattering at the grain boundary and disadvantageously low electron mobility.

While various techniques have been proposed to achieve large grain size for low-temperature polycrystalline silicon, as well as control of position of the crystal grains formed, these proposed techniques have been unsatisfactory, particularly when utilized for mass production. In connection with these various proposed techniques, note the paragraph bridging pages 4 and 5 of Applicants' specification.

Against this background, Applicants have found structure, and a technique for forming this structure, which, rather than attempting to form large grains, positively uses the crystal grain boundary itself as the active region. That is, focusing on that a plurality of crystal grains may be bonded under the joining condition having no mutual dangling bond in the {111} twin of the Diamond structure, this structure can be used as the channel part forming the active region of, for example, a thin film transistor. Note the paragraph bridging pages 5 and 6 of Applicants' specification.

That is, rather than avoiding grain boundaries, Applicants utilize specific grain boundaries (that is, twin boundaries) of a specified structure, for achieving relatively high electron mobility. Note, for example, the paragraph bridging pages 13-15 of Applicants' specification.

In addition, Applicants have found that the desired structure can easily be provided utilizing a seed crystal metal which, for example, can be retained in the

formed structure. In addition, processing can be facilitated according to the present invention wherein, for example, a same metal can be utilized both for gate electrodes and for the seed crystal metal of the present invention.

Moreover, high carrier mobility can be achieved wherein the semiconductor thin-film layer which is crystallized has a bottle-neck region (see pages 22-24 and 24-25 of Applicants' specification); or wherein dendrite crystal structure extends between the source and drain regions, through the channel region (see, e.g., pages 16-18 of Applicants' specification).

Yamazaki, et al. discloses a method of manufacturing a semiconductor device using a semiconductor thin film. This patent discloses use of a catalytic element for facilitating crystallization, which is selectively added in an amorphous silicon film, forming an added region, with a heat treatment being carried out thereafter to form a crystalline silicon film extending from the added region. This patent discloses that the crystallization temperature of the amorphous silicon film can be lowered by 50°-100°C by action of the catalytic element, and the time required for crystallization can also be reduced to 1/5 to 1/10. See column 1, lines 35-46. Note also column 4, line 48 to column 5, line 1. This patent discloses that the crystallization of the amorphous silicon film 3 (note Figs. 1A-1E) progresses first from nuclei generated in a region (nickel added region) 106 added with nickel, so that a crystal region (lateral growth region) 107 grown almost parallel to the surface of the substrate 101 is formed; and since respective crystal grains in the lateral growth region 107 are gathered in a comparatively uniform state, the lateral growth region has a merit that the total crystallinity is superior. This patent further discloses that after the crystallizing step is ended, phosphorus is added to remove nickel remaining in the lateral growth region. Note column 5, lines 7-17, 26-28, 41-48 and 57-59. Note also

column 6, lines 20-24. See further column 7, lines 21-26. Note also column 11, lines 1-45, describing orientation with respect to the crystalline silicon film. See also column 14, line 27 to column 15, line 15, describing that thin film transistor characteristics and circuit characteristics depend mainly on use of semiconductor thin films having continuity of crystal lattices at the crystal grain boundary, as the active layer of the transistor.

Initially, it is emphasized that according to Yamazaki, et al., the, e.g., nickel which is the catalytic element for the lateral growth region is gettered (removed) after formation of the lateral growth region. It is respectfully submitted that the teachings of this reference would have neither disclosed nor would have suggested the device including the seed crystal metal as in various of the present claims.

In addition, it is respectfully submitted that Yamazaki, et al. discloses random grain boundaries without limitation of number of grain boundaries, as shown in Figs. 12A and 12B thereof, and would have neither taught nor would have suggested the crystal orientation {111} of twin crystals according to the present invention, much less that good matching can be achieved at the center of the crystal structure by such crystal orientation, providing advantages of improved carrier mobility and speed as in the present invention.

Comments by the Examiner with respect to grains joined by {111} twin boundaries, in Yamazaki, et al., the Examiner pointing to column 14, lines 42-67, are noted. It is respectfully submitted, however, that Yamazaki, et al. as a whole describes random grain boundaries, without limitation of the number of grain boundaries, as shown in Figs. 12A and 12B thereof. It is respectfully submitted that Yamazaki, et al. does not disclose advantages through use of the oriented twin boundary structure, as in the present invention.

It is respectfully submitted that the additional teachings of Owyang, et al. would not have rectified the deficiencies of Yamazaki, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Owyang, et al. discloses re-entrant geometry gate electrodes for integrated circuit structures, formed by selective implantation into, e.g., polysilicon for a gate electrode, prior to etching to form the re-entrant gate electrode structure. Note column 1, lines 8-14. The species implanted is a species which will not introduce a dopant into the polysilicon. After the implantation, the implanted polysilicon layer is then subjected to an etch, preferably an anisotropic etch, which will remove the unmasked implanted portions of the polysilicon layer, as well as the implanted regions beneath the mask, resulting in a gate electrode with re-entrant or tapered walls. See column 1, line 48 to column 2, line 6.

Initially, it is respectfully submitted that the teachings of Owyang, et al. are not properly combinable with the teachings of Yamazaki, et al.

Thus, Yamazaki, et al. is concerned with manufacturing thin film semiconductor devices with facilitated crystallization of the silicon, while Owyang, et al. is concerned with the process for forming re-entrant geometry for gate electrodes. Owyang, et al. requires a polycrystalline silicon gate electrode. In view of differences in the purposes of these two patents, and methods occurring in each, it is respectfully submitted that one of ordinary skill in the art concerned with in Yamazaki, et al. would not have looked to the teachings of Owyang, et al. In other words, it is respectfully submitted that these two references are directed to non-analogous arts.

In any event, again noting differences in the procedures utilized in each, it is

respectfully submitted that the Examiner has not established any proper motivation for combining the teachings of Yamazaki, et al. and Owyang, et al., as applied by the Examiner.

Even assuming, arguendo, that the teachings of Yamazaki, et al. and Owyang, et al. were properly combinable, it is respectfully submitted that the combined teachings of these references would have neither disclosed nor would have suggested the presently claimed subject matter, including aspects thereof as discussed in the foregoing, such as crystal grain boundaries of {111} twin of Diamond structure in the recited transistor, and/or dendrite crystal regions, and/or seed crystal metal retained in the device formed, and/or bottle-neck, and advantages achieved thereby in higher electron mobility in a low-temperature polycrystalline layer.

The contention by the Examiner that the prior art discloses all subject matter but a polysilicon active layer crystallized by an agent from group IV elements, the Examiner pointing to column 2, lines 45-50, is noted. The Examiner is respectfully requested to indicate in which U.S. patent that the referred-to column 2, lines 45-50, appears.

Moreover, it is noted that Applicants use various seed crystal metals for crystallizing the semiconductor thin-film layer of Type-IV. Accordingly, basis for the conclusion by the Examiner that it would have been obvious to use group IV elements "to crystallize the active layer of the TFT of Yamazaki, [et al.] since Group IV elements are as good conductors as the typically used conductors", is not understood. The Group IV elements, for example, silicon, of Owyang, et al., are semiconductor materials, not typically used conductors. These implanted Group IV elements in Owyang, et al. are to damage the crystalline structure; and it is

respectfully submitted that Owyang, et al. would have neither taught nor would have suggested "good conductors" as implanted elements, or seed crystal metals as in the present claims.

In any event, such implanted elements in Owyang, et al., even if good conductors, would have neither disclosed nor would have suggested the crystallizing according to the present invention, providing the structure according to the present invention; and, in particular, the seed crystal metal as in various of the present claims, and crystal orientation of twin crystal, and advantages thereof.

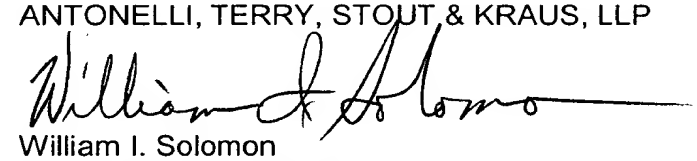
In view of the foregoing comments and amendments to the claims, reconsideration and allowance of all claims remaining in the application are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. This marked-up version is on the attached page which is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 520.39251X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel claims 1-3, 11, 16-18 and 34, without prejudice or disclaimer, and amend the claims remaining in the application as follows:

30. (Amended) A thin-film semiconductor integrated circuit device comprising a semiconductor thin-film layer provided at the upper part of an insulator, a plurality of insulated- gate [type] semiconductor elements formed at said semiconductor thin-film layer, each of said semiconductor elements having a gate electrode separated from said semiconductor thin-film layer by a gate insulating film at the surface of said semiconductor thin-film layer, and a seed crystal metal located between at least two of said gate insulating films and provided on the surface of said semiconductor thin-film layer except for the areas just under said gate insulating films.

32. (Amended) A thin-film semiconductor integrated circuit device, comprising a semiconductor thin-film layer provided at the upper part of an insulator and a plurality of insulated-gate [type] semiconductor elements formed at said semiconductor thin-film layer, wherein a portion of said semiconductor thin-film layer located between said semiconductor elements is provided with a bottle-neck region of which cross-sectional area is smaller than that of [the] other portions of said semiconductor thin-film layer.